FIGURE 1 -- PROGRAMMABLE PULSE SEQUENCER
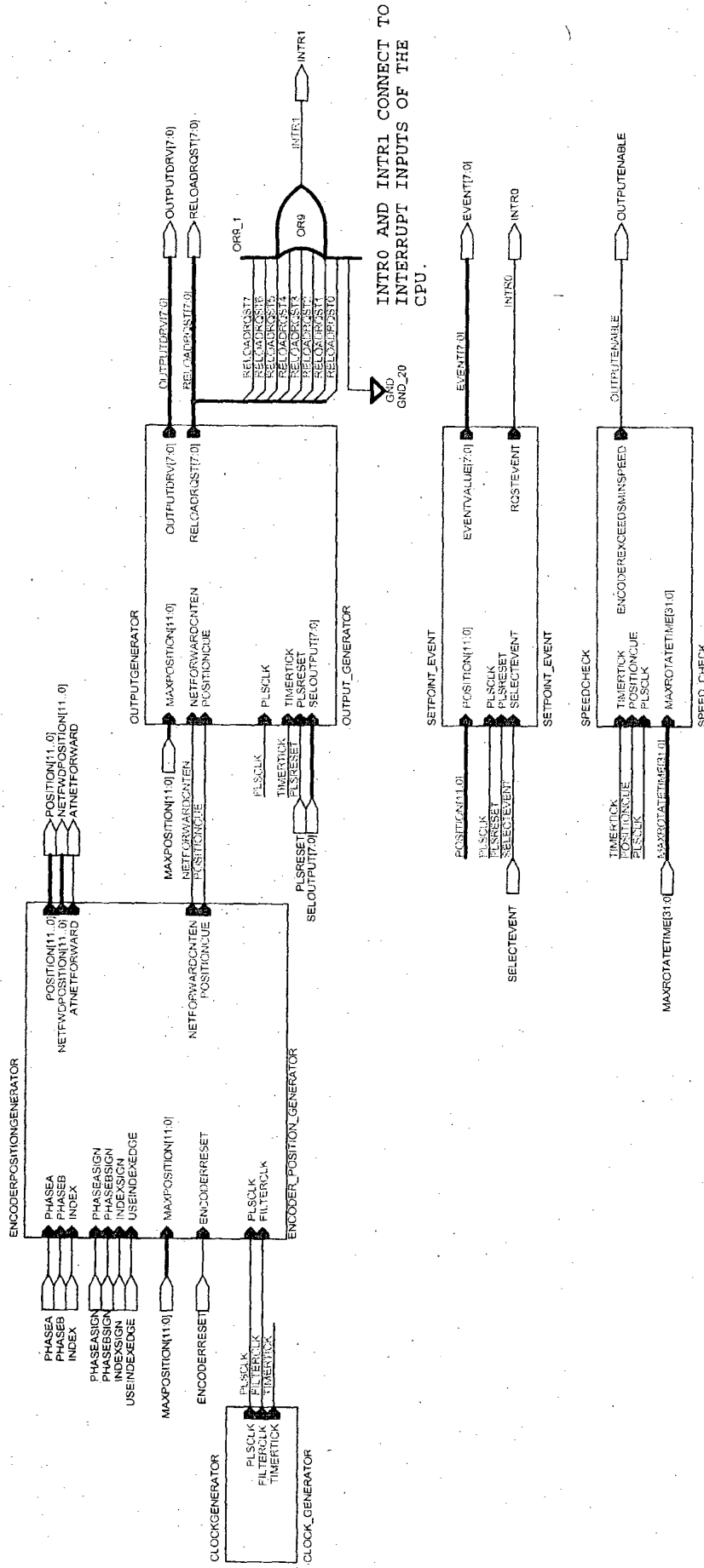

INTR0 AND INTR1 CONNECT TO
INTERRUPT INPUTS OF THE
CPU.

FIGURE 2 -- CLOCK GENERATOR

BUS CLOCK
(FROM PROCESSOR)
NOMINAL 40 MHz

FIGURE 3 -- ENCODER POSITION GENERATOR

FIGURE 4 -- FAST SIGNAL DEBOUCE
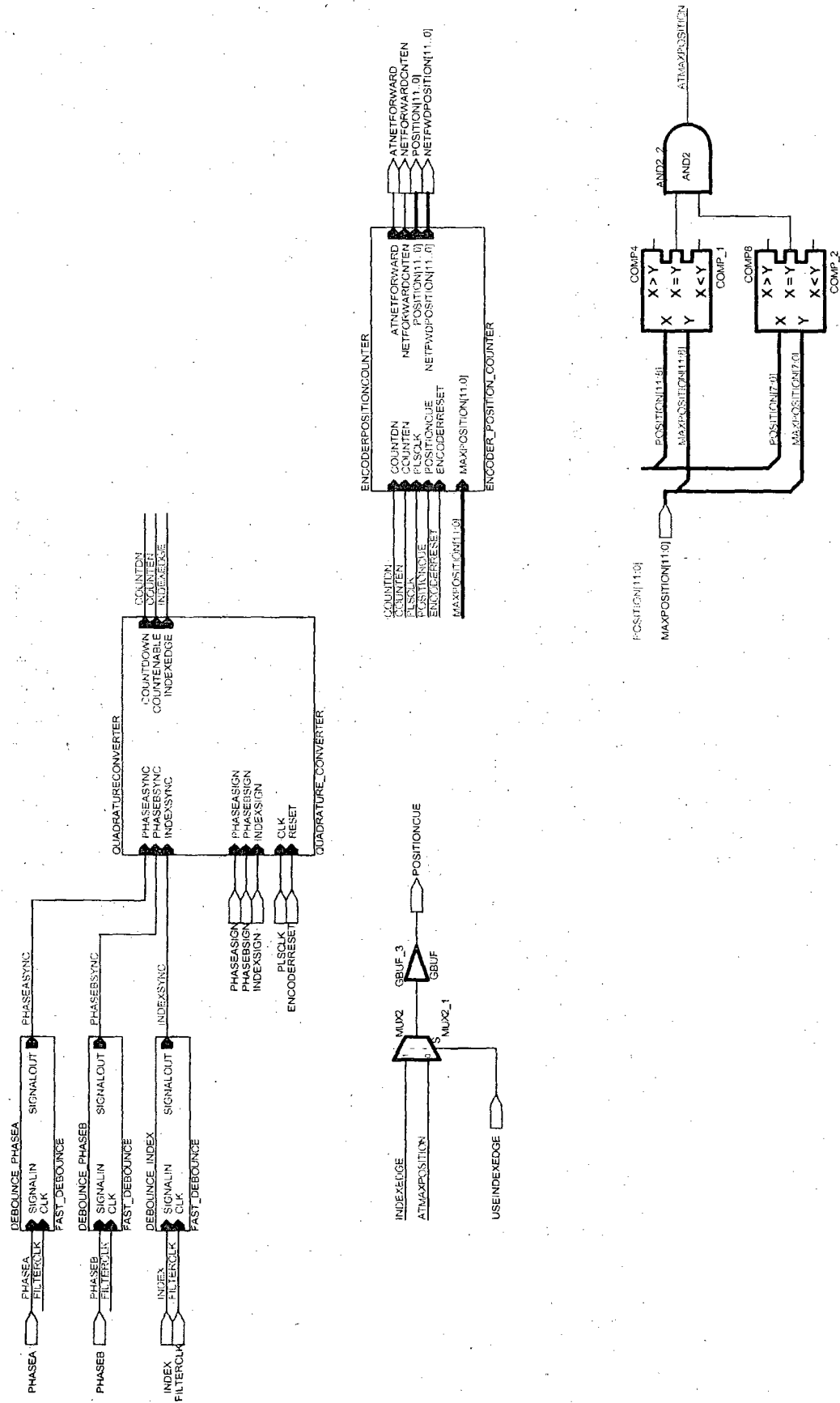
FIGURE 5 -- QUADRATURE CONVERTER

RISING EDGE DETECT
(CAN BE CHANGED TO FALLING
EDGE DETECT BY 'INDEXSIGN')
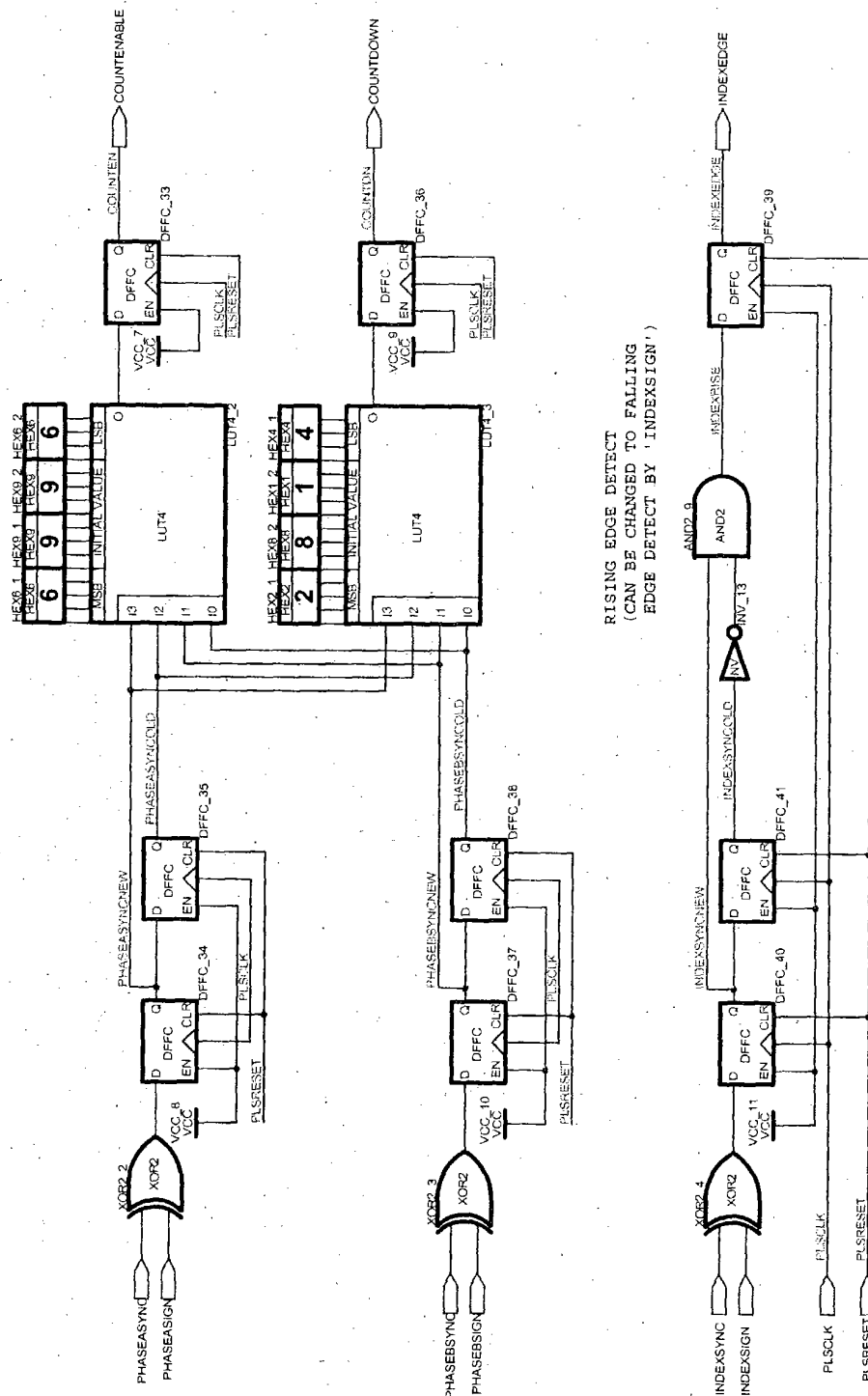
FIGURE 6 -- ENCODER POSITION COUNTER WITH NET FORWARD POSITION REGISTER

FIGURE 7 -- POSITION MULTIPLEXOR
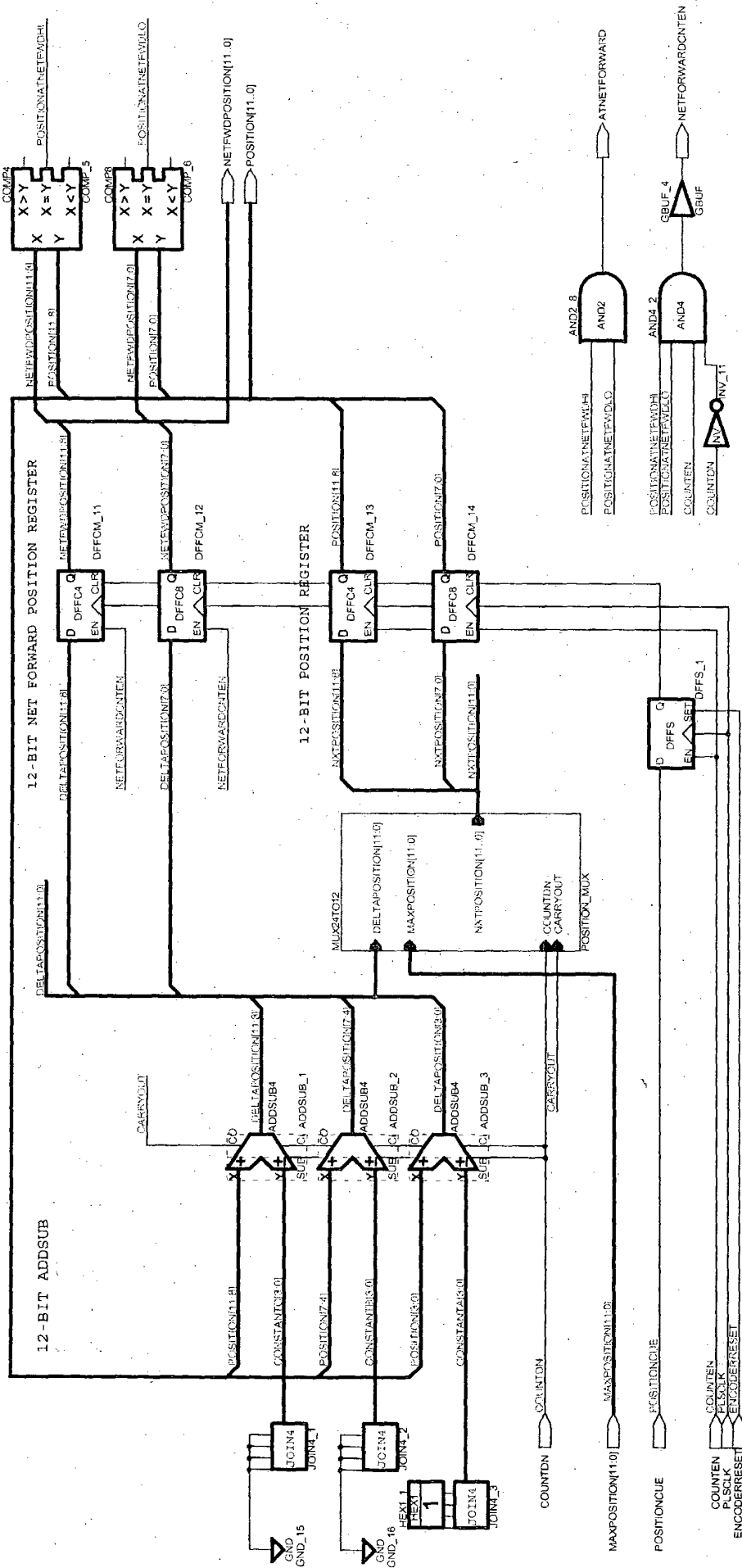
FIGURE 8 -- OUTPUT GENERATOR
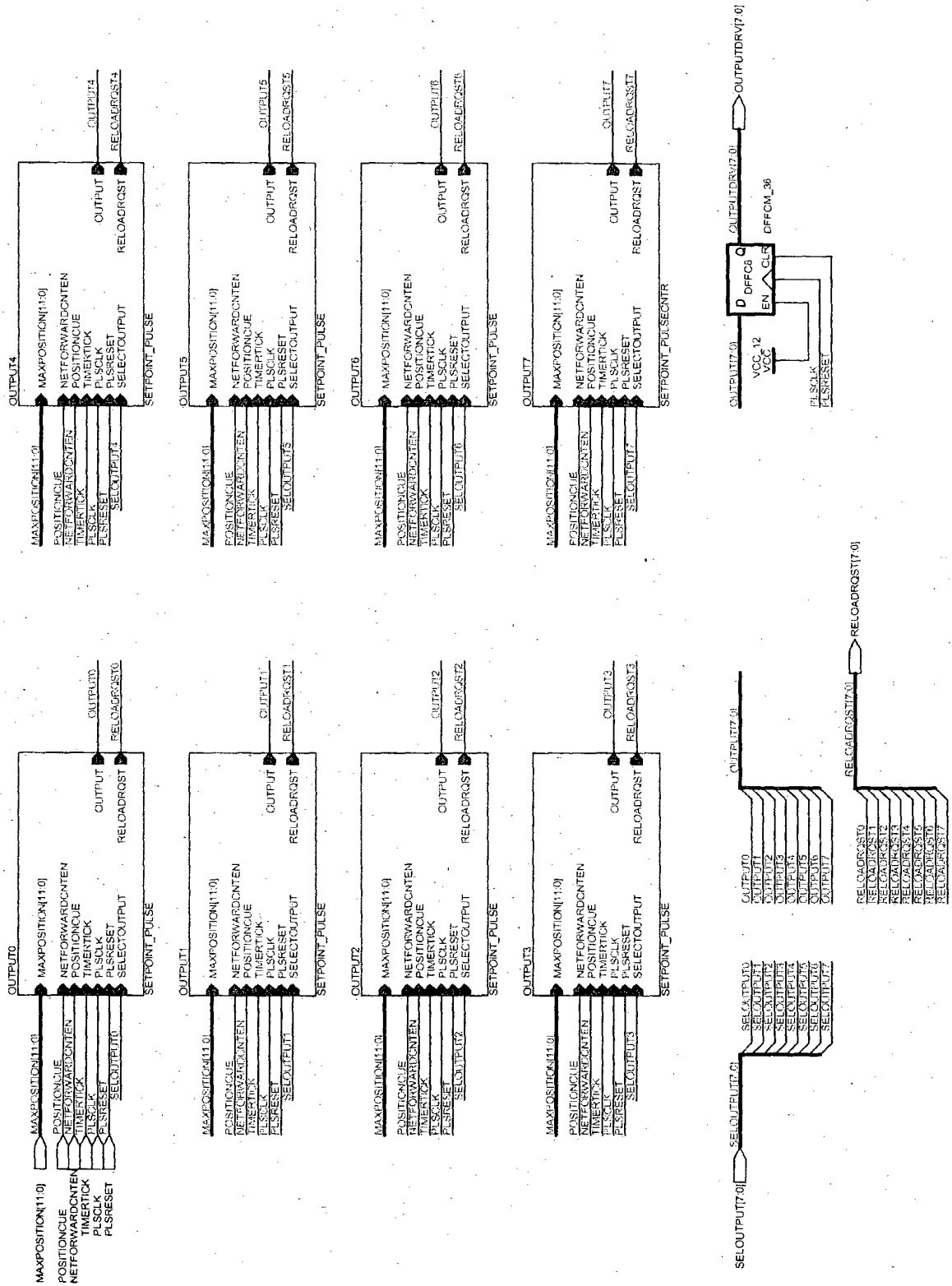
FIGURE 9 -- SETPOINT PULSE MODULE

FIGURE 10 -- OUTPUT POSITION COUNTER

PROCESSOR ADDRESS BUS

OFFSET REGISTERS --
ADDRESSES 12 TO 13

PROCESSOR DATA BUS
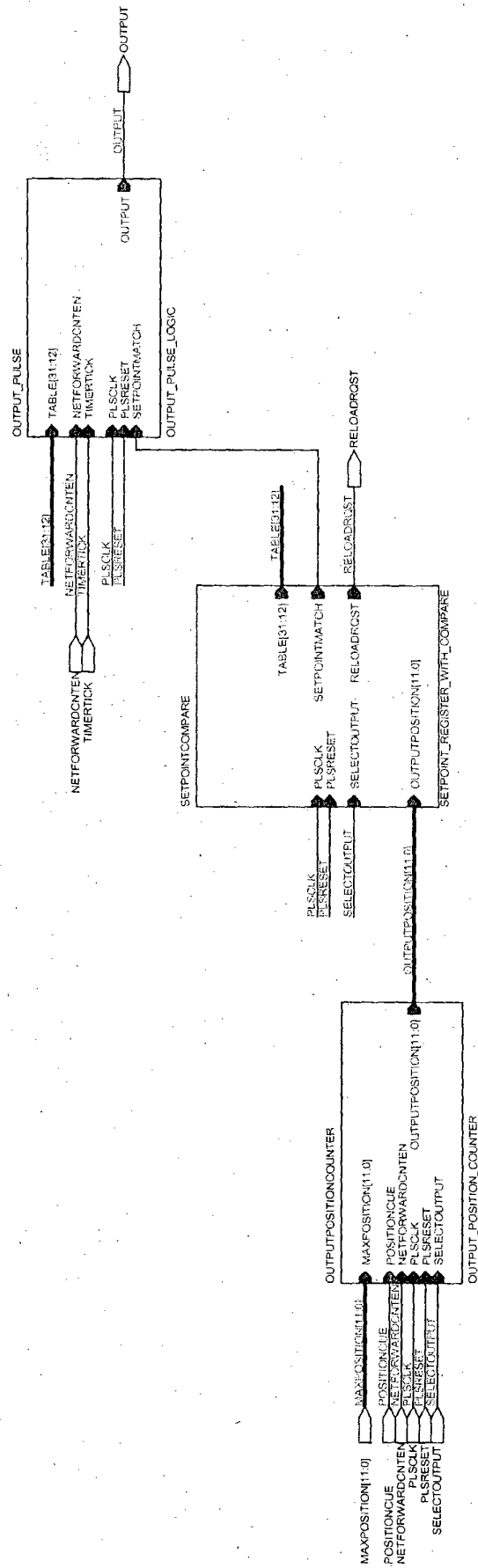
FIGURE 11 -- SETPOINT REGISTER WITH COMPARE

FIGURE 12 -- OUTPUT PULSE LOGIC

NEXT COUNT REGISTER

PULSE DOWNCOUNTER

OUTPUT MUX

NEXT COMMAND REGISTER   OUTPUT COMMAND REGISTER

FIGURE 13 -- OUTPUT PULSE LOGIC WITH ADJUSTABLE WIDTH

NEXT COUNT REGISTER   WIDTH ADJUST ADDER   PULSE DOWNCOUNTER

NEXT COMMAND REGISTER   OUTPUT COMMAND REGISTER   OUTPUT MUX

PROCESSOR DATA BUS   PROCESSOR ADDRESS BUS

WIDTH ADJUST REGISTERS --
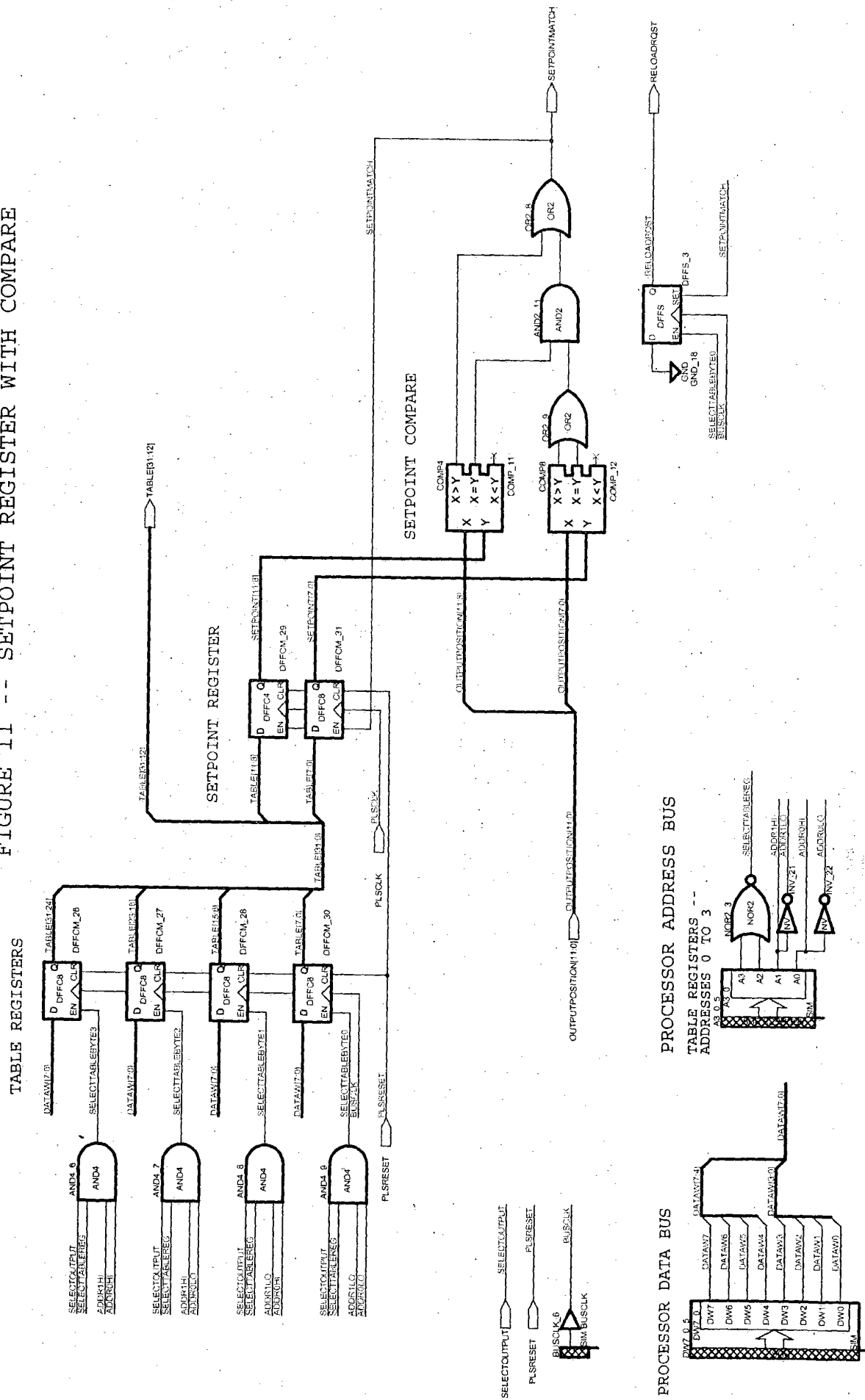ADDRESSES 14 TO 15

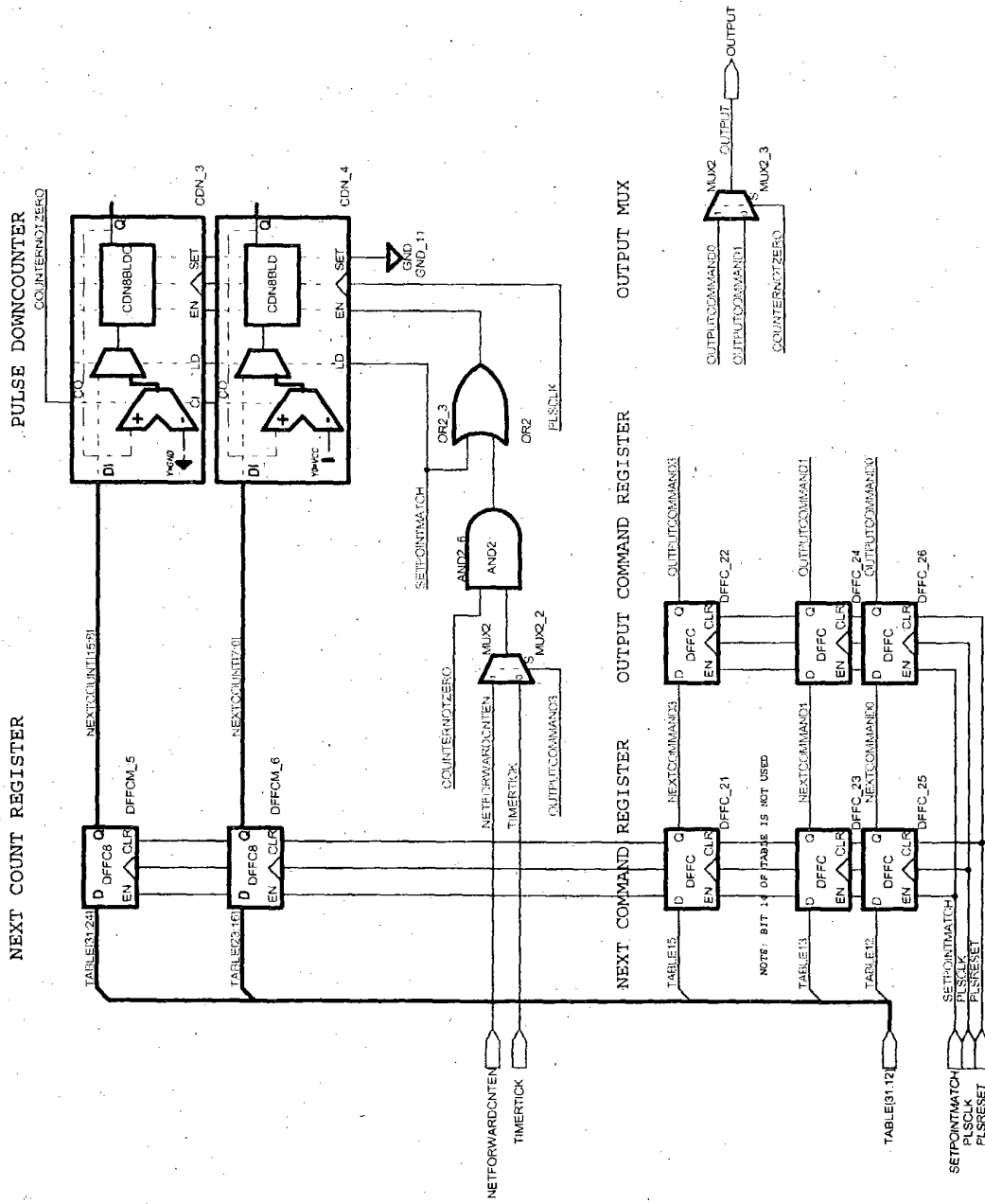# FIGURE 14 -- SETPOINT PULSE MODULE WITH OUTPUT PULSE COUNTER

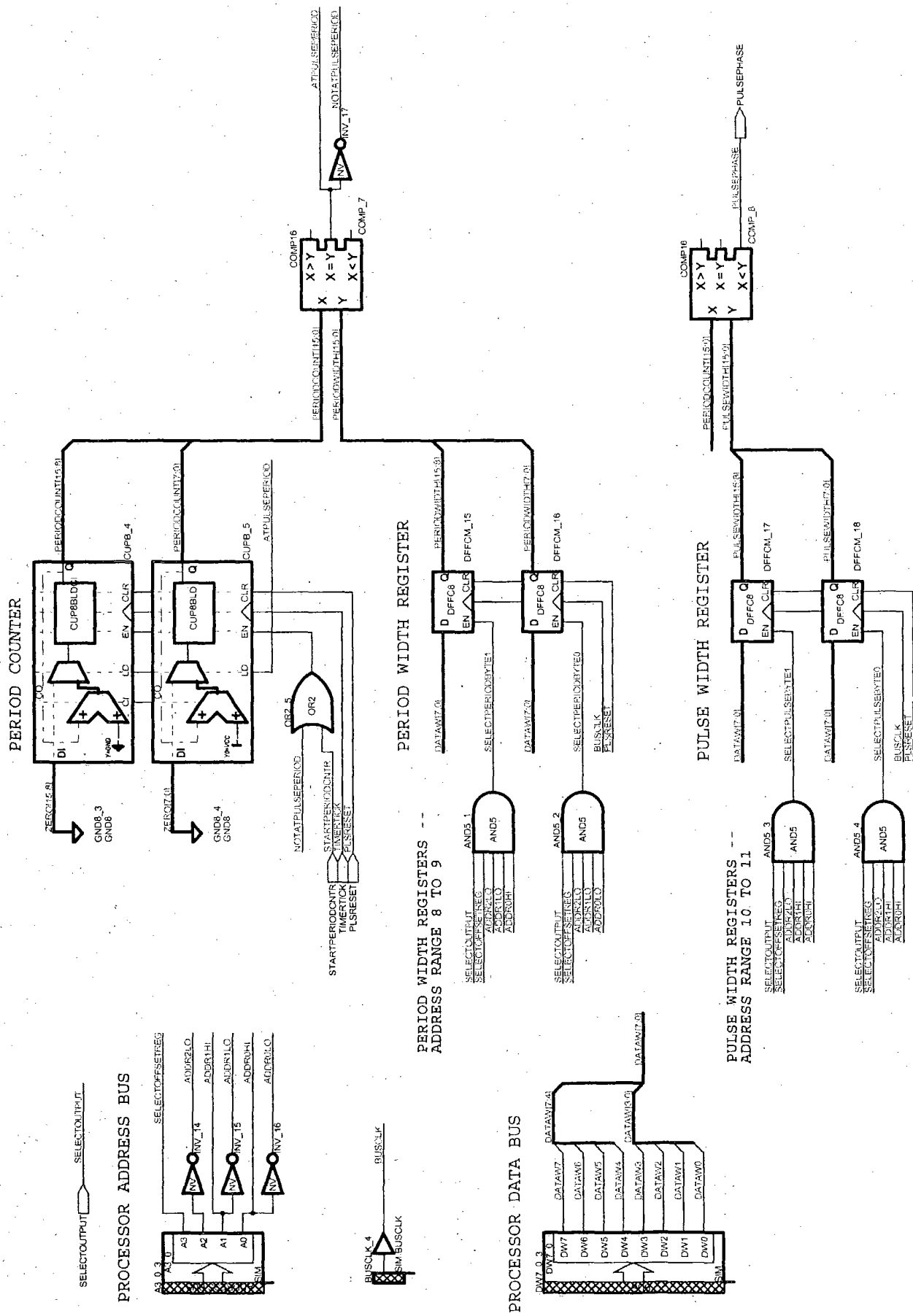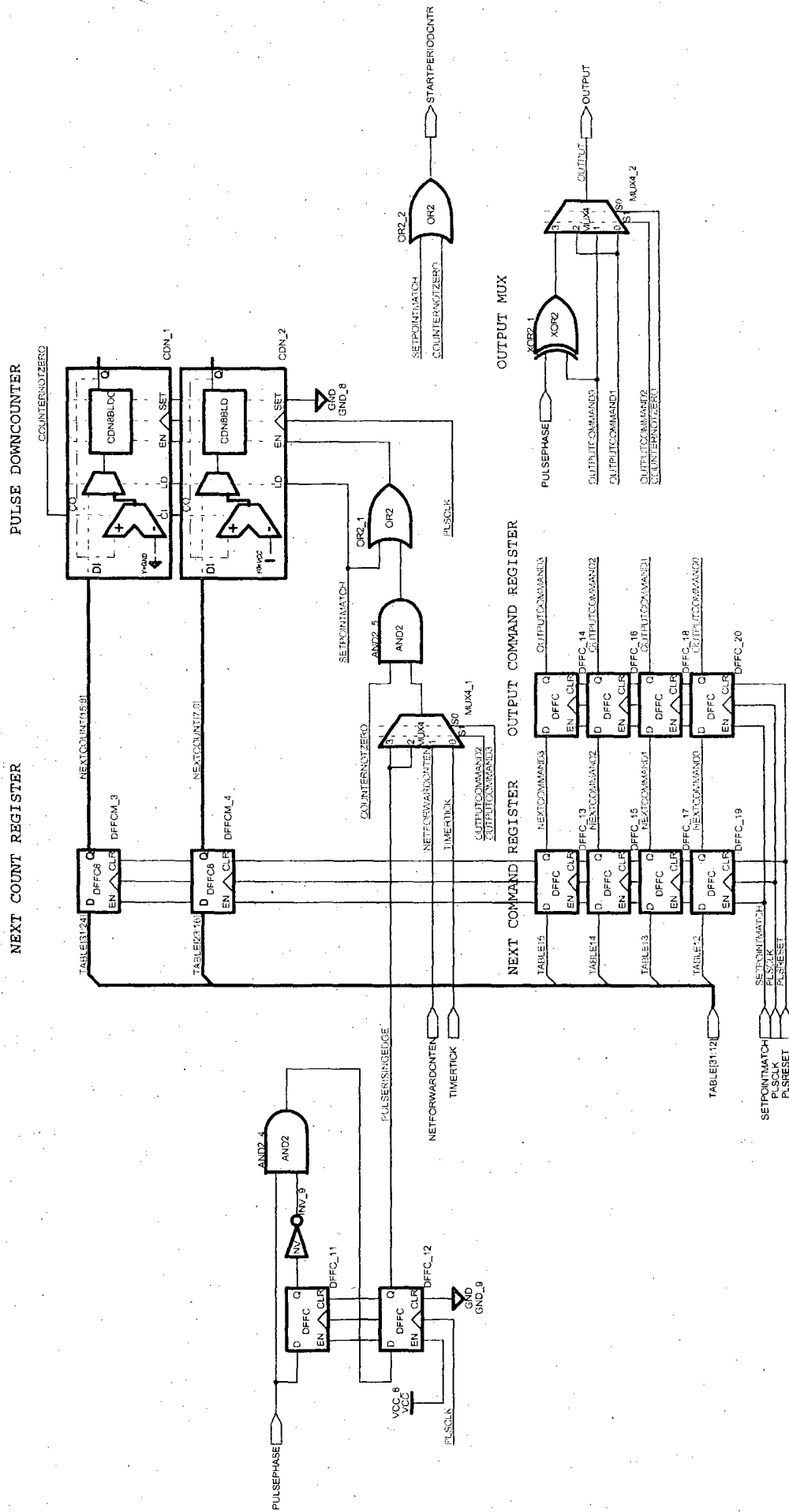# FIGURE 15 -- REPEAT PULSE GENERATOR
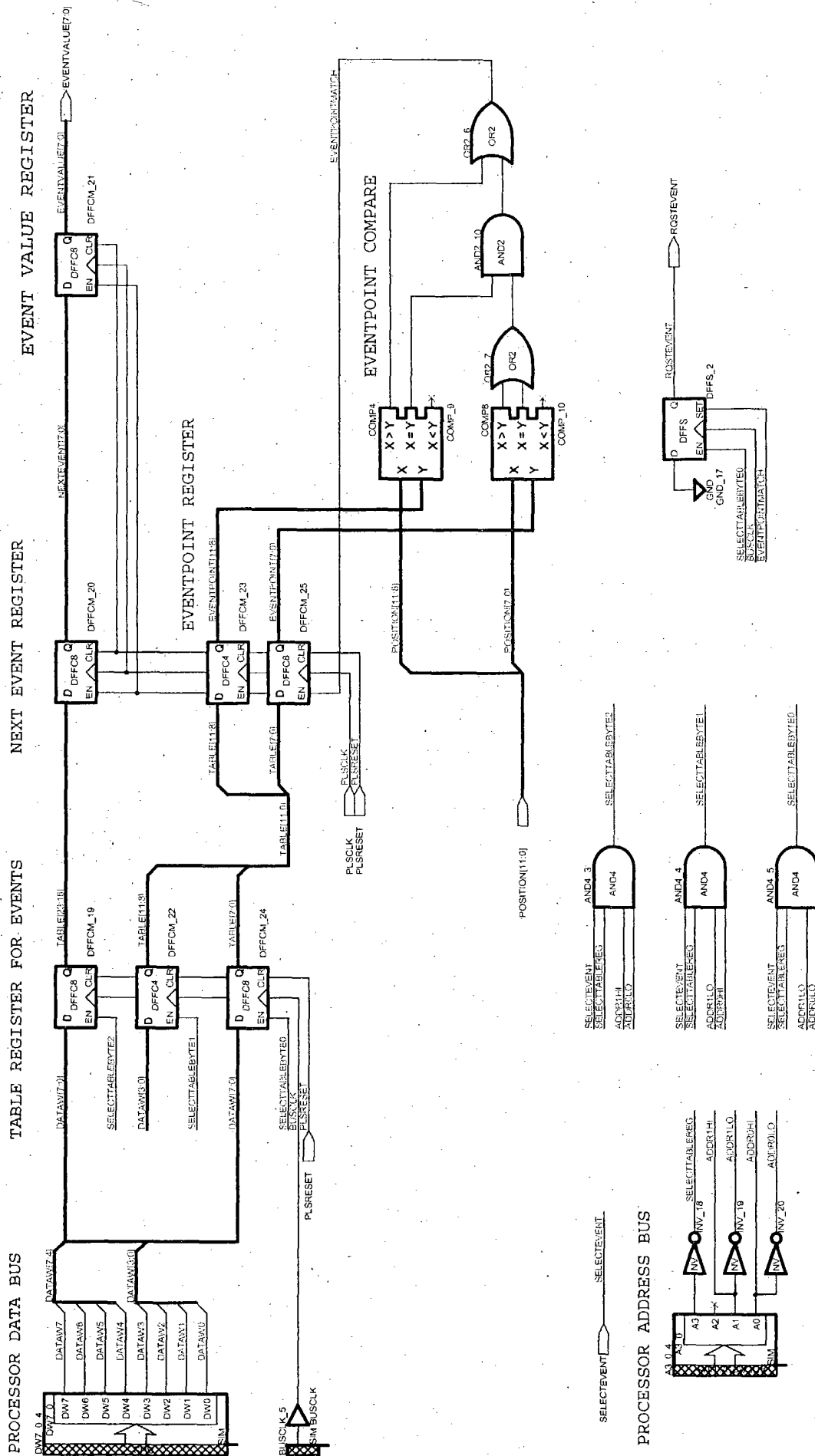
FIGURE 16 -- OUTPUT PULSE CNTR LOGIC

FIGURE 17 -- SET POINT EVENT

FIGURE 18 -- SPEED CHECK MODULE